S.V.K.P. & Dr. K.S. RAJU ARTS & SCIENCE COLLEGE
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(Affiliated to ADIKAVI NANNAYA UNIVERSITY - Recognised by Govt. of Andhra Pradesh)
PENUGONDA-534 320, West Godavari District., (A.P.)

Department of Electronics, B.O.S Meeting
Academic Year – (2025-2026)

The Meeting of the board of Studies in Electronics is held on 15-10-2025 at 10.00 A.M. in the department of Electronics.

Members Present:-

S.No.	Name	Designation
1.	Dr. Y.V.V. Appa Rao, Principal S.V.K.P & Dr.K.S.Raju A&S College,Penugonda. mail id: svkp.penugonda@gmail.com Cell: 9704448889	Chairman
2.	Dr. Ch.Kanaka Rao, Principal Head of the Electronics Department, Sri.Y.N.College(A),Narasapuram. mailid:chintapalli.kanakarao@gmail.com Cell: 9848943943	University Nominee
3.	Mr. K.S.V Sambasiva Rao, Lecturer in Electronics, PB Siddhartha Arts & Science College,Vijayawada. mail id: sambakoka@gmail.com Cell: 9441469690	Subject Expert

4.	Mr.v.Ratna sekhar HOD , Department of Electronics, D.N.R college(A),Bhimavaram mail id: dnrcollege.electronics@gmail.com Cell: 9704233301	Subject Expert
5.	Mr. G.D.SRINIVASA REDDY Lecturer in Electronics, S.V.K.P &Dr.K.S.Raju A & S College,Penugonda. mail id: dreams.gd@gmail.com cell : 8801835321	Member
6.	Ch.srinivasa rao Lecturer in Electronics, S.V.K.P &Dr.K.S.Raju A & S College,Penugonda. Mail.id :srinu.apache@gmail.com Cell: 8500495938	Member
7.	Mr. T.Naga Ratna Reddy, Lions LED Lighting Industries,Penugonda. mail id: geetharatthn@gmail.com cell : 9989880112	Industrialist /Academician
8.	Mr. P.Satya Srinivas, Lecturer in Physics, S.V.K.P & P.V Juniour College,Penugonda. mail id: srisuji.phy@gmail.com cell: 9908864413	Alumni

S.V.K.P &DR.K.S.RAJU ARTS & SCIENCE COLLEGE (A), PENUGONDA

Agenda :-

1. To frame the syllabus, Blue print and model question paper (Theory & practical) for semester v Of third year of the Academic year 2025-2026.for the admitted batch 2023-2024.

2. To frame the syllabus, Blue print and model question paper (Theory & practical) for semester I&II Of first year for the Academic year 2025-26 for the admitted batch 2025-26.

3. To discuss about the ratio of CIA(continuous internal assessment)and SEE(semester end examinations) from the present ratio 30:70 to 40:60 for 2025 -26 admitted batch onwards.

4.To coordinate teaching , research,extension and other academic activities in the department.

5. To suggest innovative teaching methods

6. To submit proposal for conducting seminars ,workshops etc.

7.To prepare syllabus for certificate or / add on programmes.

8. To prepare a list of examiners for paper setting and valuation of papers .

9.Any other matter.

Resolution:

1. Discussed and recommended that no changes are required in the proposed syllabi, Blue Print and Model Question papers for both External and Internal Examinations of Semester V for the admitted batch 2023-24.
2. Discussed and recommended that no changes are required in the proposed syllabi, Blue Print and Model Question papers for both External and Internal Examinations of Semester I and II for the admitted batch 2025-26.
3. It is resolved to change the ratio of CIA(Continuous Internal Assesment) and SEE(Semester End Examination) from the present ratio 30:70 to 40:60 for 2025-26 Admitted Batch onwards.
4. Faculty of the Department are advised to concentrate on Research work and Extension Activities by attending Seminars, Workshops and Guest Lectures etc.
5. Faculty of the Department are advised to use more ICT methods.

6. It is resolved to send proposals to UGC or any other funding agency for National Seminar/ Workshops etc.
7. Resolved to approve the syllabus for certificate/add on programmes.
8. It is resolved to approve the list of examiners prepared.

1.	Dr. Y.V.V. Appa Rao, Principal S.V.K.P & Dr.K.S.Raju A&S College,Penugonda. mail id: svkp.penugonda@gmail.com Cell: 9704448889	Chairman	
2.	Dr. Ch.Kanaka Rao, Pricipal Head of the Electronics Department, Sri.Y.N.College(A),Narasapuram. mailid:chintapalli.kanakarao@gmail.com Cell: 9848943943	University Nominee	
3.	Mr.v.Ratna sekhar HOD in department of electronics D.N.R. college (A),Bhimavaram. Mail.id :- dnrcollege.electronics@gmail.com Cell:- 9704233301	Subject Expert	
4.	Mr. K.S.V Sambasiva Rao, Lecturer in Electronics, PB Siddhartha Arts & Science College, Vijayawada. mail id: sambakoka@gmail.com Cell: 9441469690	Subject Expert	
5.	Mr. G.D.SRINIVASA REDDY Lecturer in Electronics, S.V.K.P &Dr.K.S.Raju A & S College, Penugonda. mail id: dreams.gd@gmail.com cell : 8801835321	Member	
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DEPARTMENT OF ELECTRONICS

2025-2026

Dr.Y.V.V Appa Rao chairman, BOS Electronics requests the Academic council to consider and approve the Minutes of Board of studies for the Academic Year 2025-2026 as it's BOS meeting held on 15-10-2025.

The resolutions were seconded by Dr.CH.kanaka Rao Principal sri Y.N.college (A) (Narasapuram) University Nominee of Board of studies.

The Academic Council is also requested to accord permission to appoint examiners for Theory/Practical for the Academic Year 2025-2026.

(University Nominee) (Subject Expert)

(Subject Expert) (Head Of the Department)

The blueprint for Internal examination question paper for UG Electronics

4 questions to be answered out of 6 questions

Each question carries 5 marks

Mid -term examination – I

Unit	No. of Questions	Co-CurricularActivity	Extra-CurricularActivity	Total Marks
Unit I	2	5	5	30
Unit II	2			
Unit III	1			

Mid- term examination – II

Unit	No. of Questions	Co-CurricularActivity	Extra-CurricularActivity	Total Marks
Unit III	1	5	5	30
Unit IV	2			
Unit V	2			

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SEMESTER-V

COURSE 12: CELLULAR MOBILE COMMUNICATION

Theory Credits: 4 5 hrs/week

The students will learn:

a. basics of digital cellular system, cordless telephony and cell structure

b. GSM wireless protocol and markup language fundamentals

c. basics of WLL and Bluetooth technology

UNIT-I

Advanced mobile phone service - Global system for mobile communication - Digital cellular system -Cordless telephony - Third generation wireless systems

UNIT-II

7 Cell structure - Hand off - roaming management - Hand off detection - Channel assignment techniques - Interference - ACI, CCI - Intersystem hand off and authentication - Network signaling - Cellular digital packet data

UNIT-III

GSM - Network signaling, mobility management, short message service - International roaming, administration and operation.

UNIT-IV

WAP model –WAP gateway-WAP protocol-architecture –Wap ua prof and caching- WAP developer tool kits - mobile station application executive environment.

Additional topic :- Datagram

UNIT-V

Third generation mobile services - Wireless local loop - Bluetooth technology.

Additional topic: - Distinguish between Bluetooth and Wi Fi

Text Books :-

1. Mobile Communications - Jochen Schiller, 7/e, Pearson Education, 2003.
2. Principles of Wireless Networks - Kauch Pahalavan & Prahanet Krishnamurthy, 2/ e, Pears on Education, 200 4.

Reference Books :-

1. Wireless and Mobile Networks Architecture - Yi-Bing Lin & Imnch Chlantee, John Wiley, 200 1.
2. Wireless and Mobile Communicatio n - Rapparport, Pears on Education, 20 0 1

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FIFTH SEMESTER END EXAMINATIONS

III B.Sc. –ELECTRONICS –MAJOR1/MINOR 1

CELLULAR MOBILE COMMUNICATIONS (23ELE51)

w.e.f 2023-34 Admitted BatchMODEL PAPER

Time : **3hours** Max.Marks:**70M**

Answer any five questions from Section A& Section B choosing atleast two from each section.

Eachquestion carries 10 marks. 5x10=50 marks

Part – 1

Section-A

1) Explain the architecture and working of Advanced mobile phone services (AMPS) ?
2) What are the functional differences between 1G,2G, 3G cellular networks?
3) Define handoff? Discuss in detail types of handoff, detection methods in Cellular systems?
4) Explain different types of interferences for a cellular system?
5) Explain the GSM network and signaling functions with neat diagrams?

Section-B

6) Write a note on GSM mobility management and international roaming?

7) Explain the wireless application protocol (WAP) architecture and It's components?

8) Describe the functions and components of WAP gate way and their role in Mobile communication?

9) Explain the architecture of Bluetooth and Explain the working of different blocks?

10) Explain the architecture of 3G cellular systems with neat diagram?

Part – 2

SECTION- C

Answer any five questions. **5x4=20marks**

11) What is cordless telephony?

12) Write a short note on cellular digital packet data (CDPD) ?

13) What is roaming management?

14) Explain the role of short message service (SMS) in GSM ?

15) What is international roaming?

16) Write a note on datagram?

17) write a short note on digital cellular systems ?

18) Distinguish between Bluetooth and Wi – Fi ?

Practical Paper

Work load: 30 Hrs per semester 2hrs\Week.

Minimum of 6 Experiments to be done and Recorded.

List of Experiments :-

1) speed comparision 3G vs 4G vs 5G
2) wireless application protocol (WAP) demo
3) Bluetooth communication experiment
4) cellular network basics using GSM module (sim 800L/Sim 900)
5) Sms service and network signaling
6) Wireless local loop demonstration
7) Hand off & roaming simulation
8) cell structure and frequency reuse demonstration
9) interference simulation in matlab/octave
10) sms based iot :remote sensor data via GSm

Scheme of Evaluation

Practical's :-50 Marks

Formula & Explanation:	**6**
Tabular Form+Graph+Circuit Diagram:	**6**
Observations:	**12**
Caluclation,Graph,Precautions& Result:	**6**
Viva-Voce:	**10**
Record:	**10**

The blueprint for V semester-end examination question paper for Electronics

Part-1: Answer any five questions choosing at least two from each section.

Each questioncarries 10 marks. 5x10=50 marks

Part-2: Answer any five questions.

Each question carries 4 marks. 5x4=20 marks

Unit	Part-1		Part-2	Total Marks
	Section-A	Section-B		
Unit I	2		2	28
Unit II	2		2	28
Unit III	1	1	2	28
Unit IV		2	1	24
Unit V		2	1	24
				132

(University Nominee) (Subject Expert)

(Subject Expert) (Head of the Department)

Alumni Industrialist

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SEMESTER-V

COURSE 13: COMPUTER NETWORK

Theory Credits: 4 5 hrs/week

Objective

The students will learn :

a. provides a general introduction to computer networking that would be useful to all personnel who deal with distributed systems,

b. encompassing both technical and managerial aspects.

c. to help students better understand the challenges and opportunities faced by modern business,

d. topics include LAN and WAN implementations, the Internet and internet applications.

UNIT-I

Network structure Point to Point, Broadcast, Multicast - Horizontal and vertical distribution - Star, Mesh, tree, bus structures - OSI 7 layer model - Architecture - Functions of layers - Packet switches, circuit switching and message switching.

UNIT-II

Physical layer - Transmission media - Channel allocation method s - A LOH A , S -A LOHA , FIN ITE A L OHA - L A N Protocols IEEE 80 2.3, 802 .4, 802.5, 802 .6 and 802.11.

UNIT-III

Data link layer - Framing - Error detection - Error correction - CRC - Stop and wait - Go band N - Sliding window Protocol - Selective repeat.

UNIT-IV

Network layer - Routing algorithms and congestion control algorithms - Repeaters, Bridges, Routers and Gateways, Internet working - Introduction to transport layer and session layer.

UNIT-V

Presentation layer - coding, compression and cryptography - Introduction to Application layer - High performance networks - ATM, Fast Ethernet, FDDI, DQDB, SONET and SDH.

Text Books

1. Computer Networks - Andrew S. Tanenbaum, 4/e, Pearson Education, 2005.

2. Data and Computer Communication - W. Stallings, 7/e, Pearson Education, 2006.

Reference Books

1. Introduction to Data Communications and Networking - Behrouz & Forouzan, 4/ e, M cGr aw H il l Bo ok Co m pa n y, 200 4.

2. Telecommunication Networks - Protocols Modeling and Analysis -Misha Stewartz, 2/e, Pearson Education, 2002.

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FIFTH SEMESTER END EXAMINATIONS

III B.Sc. –ELECTRONICS –MAJOR2/MINOR 2 COMPUTER NETWORKS

(23ELE52)

w.e.f 2023-34 Admitted BatchMODEL PAPER

Time : **3hours** Max.Marks:**70M**

Answer any five questions from Section A& Section B choosing atleast two from each section.

Eachquestion carries 10 marks. 5x10=50 marks

Part – 1

Section-A

1) Explain OSI 7 layer architecture with neat diagram and function of each layer**?**

2) Describe the different network topologies (star, mesh, tree, bus) with advantages and disadvantages?

3) Discuss the ALOHA? Explain about Pure ALOHA, slotted ALOHA?

4) Explain wired transmission media used in computer networks with merits and demerits?

5) Explain any three framing methods in the data link layer with examples**?**

Section-B

6) Explain the sliding window protocol and selective repeat protocol with neat diagrams?

7) Write notes on different routing algorithms used in network layer?

8) Explain the functions of the Transport layer and session layer in detail?

9) Explain the role of the presentation layer in coding, compression and cryptography?

10) Discuss ATM, Fast Ethernet and FDDI in detail?

Part – 2

SECTION- C

Answer any five questions. Each question carries 4 marks. 5x4=20marks

11) Mention any two differences between circuit switching and message switching?

12) What is the difference between broadcast and multicast?

13) What is unguided media?

14) Explain about IEEE 802.3 standard?

15) Define framing?

16) Mention two error correction techniques?

17) What is the function of a router?

18) What is SONET?

2023-2024 AB
III B.Sc., Honors in Electronics under CBCS w.e.f 2025-2026
Major -2/Minor-2 : Computer Networks
SEMESTER-V

Credits -1

List of Experiments:

1. Understanding various network tools in Windows and Linux
2. Study different types of Network devices and Cables
3. Building a Local Area Network
4. Concept of Network IP Address
5. Introduction to Network Simulator – Packet Tracer (PT)
6. Configuration of a Router using Packet Tracer
7. Implementation of a Network using Packet Tracer
8. Implementation of Static Routing using Packet Tracer
9. Implementation of RIP using Packet Tracer
10. Implementation of OSPF using Packet Tracer
11. Implement DNS using packet tracer
12. Implementation of a VLAN using Packet Tracer

Scheme of Evaluation

Practical's :-50 Marks

Formula & Explanation:	**6**
Tabular Form+Graph+Circuit Diagram:	**6**
Observations:	**12**
Caluclation,Graph,Precautions& Result:	**6**
Viva-Voce:	**10**
Record:	**10**

The blueprint for V semester-end examination question paper for Electronics

Part-1: Answer any five questions choosing at least two from each section.

Each questioncarries 10 marks. 5x10=50 marks

Part-2 : Answer any five questions.

Each question carries 4 marks. 5x4=20 marks

Unit	Part-1		Part-2	Total Marks
	Section-A	Section-B		
Unit I	2		1	24
Unit II	2		2	28
Unit III	1	1	2	28
Unit IV		2	2	28
Unit V		2	1	24
				132

(University Nominee) (Subject Expert)

(Subject Expert) (Head of the Department)

(Alumni) (Industrialist)

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SEMESTER-V

COURSE 14 A: INDUSTRIAL ELECTRONICS

Theory Credits 3 3 hrs/week

Note-1: For Semester–V, for the domain subject Electronics, any one of the above three pairs of SECs shall be chosen as courses 6 and 7, i.e., 6A & 7A or 6B & 7B or 6C & 7C. The pair shall not be broken (A, B, C allotment is random, not on any priority basis).

Note-2: One of the main objectives of Skill Enhancement Courses (SEC) is to inculcate skills related to the domain subject in students. The syllabus of SEC will be partially skill oriented. Hence, teachers shall also impart practical training to students on the skills embedded in syllabus citing related real field situations.

Learning Outcomes: Students after successful completion of the course will be able to:

1. Identify various facilities required to set up a basic Instrumentation Laboratory.
2. Acquire a critical knowledge of various Electrical Instruments used in the Laboratory.
3. Demonstrate skills of using instruments like Rectifiers, Multimeters, Power supplies,Voltage Regulators etc. through hands on experience.
4. Understand the Principle and operation of different Electronic Heating devices.

Syllabus:

UNIT-I

Rectifiers and filters: Rectifiers– Half wave, full wave and bridge rectifiers- Efficiency- Ripple factor- Regulation – Harmonic components in rectified output – Types of filters- Choke input (inductor) filter- Shunt capacitor filter- L section and section filters.

Voltage Regulators: Transistor Series voltage regulator - Transistor Shunt voltage regulator – Three terminal regulators (78XX and 79XX).

UNIT-II

Power Supplies: Block diagram of regulated power supply – A simple regulated transistorized power supply (circuit and working) – Principle and working of switch mode power supply (SMPS).

Additional topic :- Applications of SMPS

UNIT-III

Voltage Multipliers: Half wave voltage doubler, Full wavevoltage doubler, Voltage Tripler circuit diagramand working mentioning of applications of voltage multipliers.

UNIT-IV

Controlled rectifiers: SCR half wave rectifier circuit, working with wave forms, Mathematical analysis for resistive load - SCR Full wave rectifier circuit, working with wave forms, mathematical analysis for resistive load – SCR as inverter parallel and series circuits.

Additional topic :- Applications of SCR

UNIT-V

Heat effects: Resistance, inductance and dielectric heating. Principle of operations and its Applications.

Reference Books:

1. Unified Electronics Volume II by J.P Agarwal and Amit Agarwal.

2. Industrial Electronics, S.B. Biswas, Dhanapur Rai & Sons.

3. Industrial Electronics, G.K. Mithal, Khanna Publishers.48. Electronic Devices and Circuits – G.K. Mithal.

5. Electronic Devices and Circuits-Millman and Halkias- Tata Mc Graw Hill (TMH)

6. Microelectronics- J. Millman and A. Grabel – TMH

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FIFTH SEMESTER END EXAMINATIONS
III B.Sc. – ELECTRONICS – INDUSTRIAL ELECTRONICS(MAJOR3)
(23ELE53)

MODEL PAPER

Time : 3hours Max.Marks:70.

Answer any five questions from Section A & Section B choosing atleast two from each section.

Each question carries 10 marks. 5x10=50 marks

Part – 1

Section-A

1. Draw the circuit diagram of full wave rectifier and derive an expressions for Ripple factor And Efficiency?

2. Draw the circuit diagrams of Transistor Series Voltage Regulator . Explain its operations.

3. Explain the working of Regulated Transistorized power supply with neat circuit diagram.

4. Draw the Block Diagram of Switch Mode Power Supply and explain its operation.

5. Draw the circuit diagram of half wave voltage doubler circuit and explain its working.

Section-B

6. Draw the circuit diagram of Voltage Trippler circuit and explain its working.

7. Draw the circuit diagram of SCR Half wave rectifier circuit , explain its working with the help of Waveforms.

8. Draw the circuit diagram of SCR Full wave rectifier circuit, explain its working with the help of waveforms.

9. What is Dielectric heating? Explain factors on which the dielectric loss in a dielectric material

depends and mention its applications .

10. What is resistance heating? Explain its working and mention applications.

Part – 2

SECTION- C

Answer any five questions.

Each question carries 4 marks. **5x4=20 marks**

11. Distinguish between Half Wave and Full Wave Rectifiers .

12. Draw the circuit diagram of L-Section Filter and explain its working.

13. Distinguish between Linear Power Supply and SMPS .

14. Draw the block diagram of Regulated Power Supply .

15. What are different applications of Voltage Multipliers.

16. Distinguish between Half wave voltage doubler and Full wave voltage doubler .

17. Draw the circuit diagram of SCR Parallel Inverter and explain how it works ?

18. What are the applications of induction heating ?

2023-2024 AB
III B.Sc., Honors in Electronics under CBCS w.e.f 2025-2026
Major -3 : INDUSTRIAL ELECTRONICS
SEMESTER-V

(ANY SIX EXPERIMEMTS SHOULD BE DONE)

1. D.C Power supply and filters.
2. Transistor series regulator
3. Transistor as a shunt regulator
4. Voltage regulator using IC-7805and IC-7905.
5. Voltage doubler using diodes
6. Voltage Tripler using diodes
7. SCR VI characteristics.
8. SCR Series inverter
9. SCR parallel inverter.

Scheme of Evaluation

Practical's :-50 Marks

Formula & Explanation:	**6**
Tabular Form+Graph+Circuit Diagram:	**6**
Observations:	**12**
Caluclation,Graph,Precautions& Result:	**6**
Viva-Voce:	**10**
Record:	**10**

The blueprint for V-semester end examination question paper for Electronics

Part-1 : Answer any five questions choosing atleast two from each section.

Each question carries 10 marks. 5x10=50 marks

Part-2 : Answer any five questions.
Each question carries 4 marks. 5x4=20 marks

Unit	Part-1		Part-2	Total Marks
	Section-A	Section-B		
Unit I	2		2	28
Unit II	2		2	28
Unit III	1	1	2	28
Unit IV		2	1	24
Unit V		2	1	24
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COURSE 15 A: DIGITAL SYSTEM DESIGN

Theory Credits: 3 3 hrs/week

a. the fundamentals of Boolean algebra and simplification of Boolean functions

b. the combinational logic circuits and their design using HDL

c. the sequential logic circuits and their design using HDL

UNIT-I

Boolean Algebra and Logic Gates: -

Review of binary number systems - Binary arithmetic - Binary codes - Boolean Algebra and theorems - Boolean functions - Simplifications of Boolean functions using Karnaugh map and tabulation methods - Logic gates.

UNIT-II

Combinational Logic:-

Combinational circuits - Analysis and design procedures - Circuits for arithmetic operations - Code conversions - Introduction to Hardware Description Language (HDL).

UNIT-III Design with MSI Devices:-

Decoders and Encoders - Multiplexers and De multiplexers - Memory and programming logic - HDL for combinational circuits.

UNIT-IV Synchronous Sequential Logic: -

Sequential circuits - Flip-flops - Analysis and design procedures - State reduction and state assignments - Shift registers - Counters – HDL for sequential logic circuits, shift registers and counters.

UNIT-V Asynchronous Sequential Logic: -

Analysis and design of asynchronous sequential circuits - Reduction of state and flow tables - Race free state assignment - Hazards.

Text Books

1. Digital Logic and Computer Design - M. Morris Mano, Prentice Hall of IndiaPrivate Limited.

2. A Verilog HDL Premier - J. Baskar, Pearson Education.

Reference Books

1. Analysis and Modeling of Digital Systems - Zain Allabedin Navabee, 2/e , McGrawHill Publishing Co. Ltd., New Delhi.

2. An Engineering Approach to Digital Design - Fletcher, Prentice Hall of IndiaPrivate Limited.

3. Modern Digital Electronics - R.P. Jain, 2/e, Tata McGraw Hill Publishing Co. Ltd.,New Delhi.

4. Digital Fundamentals - T.L. Floyd, 8/e, Pearson E

Co-Curricular Activities

(a) Mandatory: (Training of students by teacher in field related skills: (lab:10 + field:05)

1**. For Teacher**: Training of students by the teacher in the in the laboratory/fieldfor not less than 15 hours on the field techniques/skills of understanding the operation, Maintenance and utility of various electrical and electronic instruments both in the Laboratory as well as in daily life.

For Student: Students shall (individually)visit a local electrical and electronics shop or small firm to familiarize with the various electrical and electronic instruments available in the market and also to understand their functionality, principle of operation and applications as well as the troubleshooting of these instruments.(Or) Student shall visit a diagnostic centre and observe the ECG machine and the ECG

pattern(Or) Student shall visit a diagnostic centre and observe the CT scan and MRI scan.(Or) Student shall visit a mobile smart phone repair shop and observe the different components on the PCB(Motherboard), different ICs (chips) used in the motherboard and trouble shooting of touch screen in smart phones.

Observations shall be recorded in a hand-written Fieldwork/Project work not exceeding10 pages in the given format to be submitted to the teacher.

2. Max marks for Fieldwork/Project work: 05.

3. Suggested Format for Fieldwork/Project work: Title page, student details, indexpage, details of place visited, observations, findings and acknowledgements.

4. Unit tests (IE)

Suggested Co-Curricular Activities

1. Training of students by related industrial / technical experts.

2. Assignments (including technical assignments like identifying different measuring instruments and tools and their handling, operational techniqueswith safety and security.

3. Seminars, Group discussions, Quiz, Debates etc. (on related topics).

4. Making your own stethoscope at home.

5. Making seven segment display at home.

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(Affiliated to ADIKAVI NANNAYA UNIVERSITY–Recognised by Govt. of Andhra Pradesh)
FIFTH SEMESTER END EXAMINATIONS
III B.Sc. – ELECTRONICS – DIGITAL SYSTEM DESIGN (MAJOR4)
(23ELE54)

MODEL PAPER

Time : 3hours Max.Marks:70.

Answer any five questions from Section A & Section B choosing atleast two from each section.

Each question carries 10 marks. 5x10=50 marks

Part – 1

Section-A

1. What is binary code? And explain about weighted and non weighted?
2. Simplify the following Boolean expression by using k- map
   a) F = A'B'C'D'+A'B'C'D + AB'CD'+AB'CD+ABCD'+ABCD
   b) F (A,B,C,D) =∑m(1,3,5,7)
3. What are combinational circuits? Design procedure of combinational circuit?
4. Explain introduction to hardware description language (HDL)?
5. Write about programmable logic array (PLA)?

Section -B

6. What is Decoder? And design 3x8 Decoder with logical diagram?
7. What is flip flop and Explain S-R and J-K flip flops ?
8. What is Shift register? Explain different types of shift registers ?
9. Explain design and analysis procedure of Asynchronous sequential logic circuits?
10. What is hazard and explain their types?

Part – 2

SECTION- C

Answer any five questions.

Each question carries 4 marks. **5x4=20 marks**

11. Convert the decimal number 431 to binary?

12. State demOrgan's theorem?

13. What is code conversion give one example?

14. Write about medium scale integration (MSI)?

15. Explain about combinational circuits?

16. Explain the types of Memory?

17. What is T-flip-flop?

18. What is Race free state assignment ?

2023-2024 AB
III B.Sc., Honors in Electronics under CBCS w.e.f 2025-2026
Major -4 : DIGITAL SYSTEM DESIGN
SEMESTER-V

Credits -1

List of Experiments:

1 Design and hardware implementation of 3:8 Decoders (using NAND gates)

2. Realization of R-S, D, J-K latches and D flip-flop using NAND gates only

3. Realization of Mod 8 up-down ripple counter.

4. Realization of Mod-2 and Mod-3 Synchronous counter.

5. Design and hardware implementation of 3:8 Encoders (using NAND gates)

6. Modeling Half-adder

7. Modeling Full-adder8

8. Construct: 4-to-1 Multiplexer

9. Consruct: 1-to-4 Demultiplexer

10. Realization of Mod-8 Up-Down Ripple Counter

Scheme of Evaluation

Practical's :- 50 Marks

Formula & Explanation:	**6**
Tabular Form+Graph+Circuit Diagram:	**6**
Observations:	**12**
Caluclation,Graph,Precautions& Result:	**6**
Viva-Voce:	**10**
Record:	**10**

The blueprint for V-semester end examination question paper for Electronics

Part-1 : Answer any five questions choosing atleast two from each section.

Each question carries 10 marks. 5x10=50 marks

Part-2 : Answer any five questions.
Each question carries 4 marks. 5x4=20 marks

Unit	Part-1		Part-2	Total Marks
	Section-A	Section-B		
Unit I	2		2	28
Unit II	2		2	28
Unit III	1	1	2	28
Unit IV		2	1	24
Unit V		2	1	24
				132

(University Nominee) (Subject Expert)

(Subject Expert) (Head of the Department)

(Alumni) (Industrialist)

S.V.K.P. & Dr. K.S. Raju Arts & Science College (Autonomous),

PENUGONDA

I -Semester Electronics Major -1

Course1: Fundamental of Electricity and Electronics (25ELE11)

(w.e.f. 2025-26 AB)

THE BLUEPRINT FOR CIA

Section-A: Answer any three questions out of five questions.

Each question carries 6 marks. 3x6=18 marks

Section-B: Answer any three questions out of five questions.

Each question carries 4 marks. 3x4=12 marks

Mid Term Examination – I					
Unit	**Section-A**	**Section-B**	**Co-Curricular Activity**	**Extra-Curricular Activity**	**Total Marks**
Unit I	2	2	5	5	40
Unit II	2	2			
Unit III	1	1			
Total	5(3X6=18M)	5(3X4=12M)			
Mid Term Examination – II					
Unit	**Section-A**	**Section-B**	**Co-Curricular Activity**	**Extra-Curricular Activity**	**Total Marks**
Unit III	1	1	5	5	40
Unit IV	2	2			
Unit V	2	2			
Total	5(3X6=18M)	5(3X4=12M)			

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PENUGONDA-534 320, West Godavari District., (A.P.)

I Semester Syllabus w.e.f (2025-26Admitted Batch)

MAJOR AND MINOR

COURSE 1: FUNDAMENTALS OF ELECTRICITY AND ELECTRONICS

(25ELE11)

Objectives :-

The students will learn:

1) basics of electrostatics, Gauss theorem and its applications,
concept of a capacitor, various types of capacitors and dielectric constant,
magnetic effects of current, cells and the measuring instruments like ammeter and voltmeter,
1) basics of p-n junction, rectifying action of a diode, regulated power supplies and wave shaping circuits,
2) transistor and its three modes of operation, h-parameter model of a transistor and the frequency response of an amplifier.

UNIT-I Electrostatics:- (**9 hrs**)

Electric charges - Coulomb's law - Electric field - Electric intensity and electric potential- Relation between electric potential and intensity - Electric intensity and potential due to a uniform charged conducting sphere at a point outside, on and inside the conductor.

Electric dipole - Dipole moment - Intensity and potential due to a dipole – Statement and proof of Gauss law - Application of Gauss law to uniformly charged solid sphere.

UNIT-II Capacitors:- (9hrs)

Definition and unit of capacity - Capacitance of a parallel plate capacitor - Effect of dielectric on capacity - Capacitors in series and parallel - Energy stored in a charged capacitors - Loss of energy on sharing of charges between two capacitors - Force of attraction between plates of charged parallel plate capacitor - Kelvin's attracted disc electrometer - Measurement of potential and dielectric constant.

Type of capacitors - Mica capacitor, Electrolytic capacitors, Variable air capacitor – Uses Of capacitors.

UNIT-III Electrical Measurements: (9hrs)

Carey-Foster bridge - Determination of specific resistance - Potentiometer - Calibration of low and high range voltmeters - Calibration of Low rangeammeter.
Magnetic Effect of Current: Biot-Savart's law [Force on a conductor carrying current placed in a magnetic field] - Amperes law-Principle .construction and theory of a moving coil ballistic galvanometer – Measurement of figure of merit of B.G..

UNIT-IV Diode circuits and power Supplies:- (9hrs)

Junction diode characteristics - Half and full wave rectifiers - Expression for efficiency and ripple factor – Construction of low range power peak using diodes -Bridge rectifier - Filter circuits – Zener Diode – Characteristics - Regulated power supply using Zener diode .

Additional topic :- Differentiator and integrator using resistor and capacitor

UNIT-V Transistor circuits:- (9hrs)

Characteristics of a transistor in CB, CE modes - Relatively meritsGraphical analysis in CE configuration - Transistor as a amplifier - RC coupled amplifier –Frequency response -h parameters.Basis logic gates AND, OR, and NOT - Construction of basic logic gates.

Additional topic :- NAND and NOR gates universal gates

Text Books:-

1. Electricity and Magnetism - *M. Narayanamoorthi and Others*, National Publishing Co., Chennai.

2. Electricity and Magnetism - *R. Murugeshan*, S. Chand & Co. Ltd., New Delhi, Revised Edition, 2006.

3. Principles of Electronics - *V.K. Mehta*, S. Chand & Co., 4/e, 2001.

4. Basic Electronics - *B.L. Theraja*, S. Chand & Co., 4/e, 2001.

Reference Books:-

5. Electricity and Magnetism - *Brijlal & Subrahmanyam*, Ratan Prakashan Mandir,Agra.

6. Fundamentals of Electricity and Magnetism - *B.D. Duggal & C.L. Chhabra*, ShobanLal Nagin Chand & Co., Jallundur.

7. Physics, Vol. II - *Resnick, Halliday & Krane*, 5/e, John Wiley & Sons, Inc.,.

8. Basic Electronics - *B. Grob*, McGraw - hill, 6/e, NY, 1989.

9. Elements of Electronics - *Bagde & Singh*, S. Chand

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I B.Sc. –ELECTRONICS –: FUNDAMENTALS OF ELECTRICITY AND ELECTRONICS

PAPER

Time : **3hours** Max.Marks:**60M**

Answer any five questions from Section A & Section B choosing atleast two from each section.
Eachquestion carries 8 marks. 5x8=40 marks

Part – 1

Section-A

1. What is electric potential. Derive an expression for potential due to uniform charged conducting sphere ?

2. State and prove Gauss law in electrostatics and derive an expression for uniformly charged solid sphere ?

3. Derive an expression for the capacitance of parallel plate capacitor ?

4. What is capacitor? Explain the types of capacitor .Mention its uses ?

5. Determine the specific resistance from Carey forster bridge ?

Section-B

6. Explain the construction and working of Moving Coil Galvanometer
7. Explain the working of Full wave Bridge rectifier and find its ripple factor.
8. Explain the working of Differentiator and Integrator using capacitor and resistor
9. Explain the characteristics of CE configuration.?
10. Explain the construction and working of basic logic gates ?

Part – 2

SECTION- C

Answer any five questions. **5x4=20 marks**

11. Explain Coulomb's law in electrostatics.
12. Describe an expression for the energy stored in a condenser ?
13. Explain the working of serial and parallel capacitor ?
14. Explain the calibration of low range ammeter?
15. State and explain Biot Savarts law ?
16. What is P-N junction diode ? Explain its working in forward bias ?
17. Explain the regulated power supply using Zener diode?
18. Explain transistor act as amplifier ?

SEMESTER - I

COURSE 1: FUNDAMENTALS OF ELECTRICITY AND ELECTRONICS

Practical Credits: 1 2 hrs/week

List of Experiments:

1. Kirchoff's verification
2. Logic Gates – Verification of Truth Tables
3. PN Junction Diode – V-I Characteristics
4. Zener Diode – V-I Characteristics
5. Zener Diode as a Voltage Regulator
6. Carey- Fasters Bridge.
7. Series and Parallel Combination of Resistors and Capacitors
8. Bridge Rectifier – L and π filters

Scheme of Evaluation

Practical's:- **50 Marks**

Formula & Explanation:	**6**
Tabular Form+Graph+Circuit Diagram:	**6**
Observations:	**12**
Caluclation,Graph,Precautions& Result:	**6**
Viva-Voce:	**10**
Record:	**10**

THE BLUEPRINT FOR (SEMESTER END EXAMS) SEE

Part-1: Answer any five questions choosing at least two from each Section A & Section B.

Each question carries 8 marks. 5x8=40 marks

Part-2: Answer any five questions. Each question carries 4 marks. 5x4=20 marks

Unit	Part-1		Part-2	Total Marks
	Section-A	Section-B		
Unit I	2		1	20
Unit II	2		2	24
Unit III	1	1	2	24
Unit IV		2	2	24
Unit V		2	1	20
	5	5	8	112

(University Nominee) (Subject Expert)

(Subject Expert) (Head Of the Department)

(Alumni) (Industrialist)

S.V.K.P. & Dr. K.S. Raju Arts & Science College (Autonomous),

PENUGONDA

I -Semester Electronics Major -2

Course1: Circuit theory and Electronic devices (25ELE12)

(w.e.f. 2025-26 AB)

THE BLUEPRINT FOR CIA

Section-A: Answer any three questions out of five questions.

Each question carries 6 marks. 3x6=18 marks

Section-B: Answer any three questions out of five questions.

Each question carries 4 marks. 3x4=12 marks

Mid Term Examination – I					
Unit	**Section-A**	**Section-B**	**Co-Curricular Activity**	**Extra-Curricular Activity**	**Total Marks**
Unit I	2	2	5	5	40
Unit II	2	2			
Unit III	1	1			
Total	5(3X6=18M)	5(3X4=12M)			
Mid Term Examination – II					
Unit	**Section-A**	**Section-B**	**Co-Curricular Activity**	**Extra-Curricular Activity**	**Total Marks**
Unit III	1	1	5	5	40
Unit IV	2	2			
Unit V	2	2			
Total	5(3X6=18M)	5(3X4=12M)			

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PENUGONDA-534 320, West Godavari District., (A.P.)

I Semester Syllabus w.e.f (2025-26 Admitted Batch)

COURSE 2: CIRCUIT THEORY AND ELECTRONIC DEVICES (25ELE12)

Objectives:

- To explain the basic concepts and laws of DC andAC electrical networks and solve them using mesh and nodal analysis techniques.
- To analyze circuits in time and frequency domain.
- To synthesize the networks using passive elements.
- To understand the construction, working and VIcharacteristics of electronic devices.
- To understand the concept of power supply.

UNIT- 1:

SINUSOIDAL ALTERNATING WAVEFORMS:

Definition of current and voltage. The sine wave, general format of sine wave for voltage or current, phase relations, average value, effective (R.M.S) values. Differences between A.C and D.C. Phase relation of R ,L and C

UNIT-II:

PASSIVE NETWORKS AND NETWORKS THEOREMS (D.C):

Branch current method, Nodal Analysis, star to delta & delta to star conversions. SuperpositionTheorem, Thevenin's Theorem, Norton's Theorem, Maximum Power, Milliman and Reciprocity theorems .

UNIT-III:

RC, RL AND RLC CIRCUITS:

Frequency response of RC and RL circuits, their action as low pass and high pass filters. Passive differentiating and integrating circuits. Series resonance and parallel resonance circuits, Q – Factor.

Additional topic:- difference between active and passive components.

UNIT-IV:

BJT, FET and UJT:

BJT: Construction, working, and characteristics of CE Configurations. Hybrid parameters and hybrid equivalent circuit of CE Transistor,

FET: Construction, working and characteristics of JFET and MOSFET. Advantages of FET over BJT.

UJT: Construction, working and characteristics of UJT. UJT as aRelaxation oscillator.

UNIT-V:

POWER SUPPLIES & PHOTO ELECTRIC DEVICES

Rectifiers :Half wave ,full wave rectifiers-Efficiency-ripple factor- Filters- L- section & π-section filters. Three terminal fixed voltage I.C. regulators (78XX and &79XX). Light Emitting Diode – Photo diode and LDR.

Additional topic :- silicon controlled rectifier (SCR)

TEXT BOOKS:

1. Introductory circuit Analysis (UBS Publications) ---------- Robert L. Boylestad.
2. Electronic Devices and Circuit Theory ---------- Robert L. Boylestad & Louisashelsky.
3. Circuit Analysis by P. Gnanasivam- Pearson Education
4. Electronic Devices and Circuit Theory---------- Robert L. Boylestad & Louis Nashelsky.
5. Electronic Devices and Circuits I – T.L.Floyd- PHI Fifth Edition

REFERENCE BOOKS:

1. Engineering Circuit Analysis By: Hayt & Kemmerly - MG.
2. Networks and Systems – D.Roy Chowdary.
3. Unified Electronics (Circuit Analysis and ElectronicDevices) by Agarwal- Arora
4. Electric Circuit Analysis- S.R. Paranjothi- New Age International.
5. Integrated Electronics – Millmam & Halkias.
6. Electronic Devices & Circuits – Bogart.
7. Sedha R.S., A Text Book Of Applied Electronics, S.Chand & Company Ltd

Outcomes:-

- ✓ Apply concepts of electric network topology, nodes, branches,loops to solve circuit problems including the use of computer simulation.
- ✓ Apply time and frequency concepts of analysis.
- ✓ Synthesize the network using passive elements.
- ✓ Know about amplifier circuits, switching circuits and oscillatorcircuits their design and use in electronics.

Design and construction of a power supply

SEMESTER-I

COURSE 2: CIRCUIT THEORY AND ELECTRONIC DEVICES

Work load: 30 Hrs per semester 2hrs\Week.

Minimum of 2 Experiments to be done and Recorded.

List of the Experiments :-

1. Thevenin's Theorem-verification
2. Norton's Theorem-verification
3. Maximum Power Transfer Theorem-verification
4. LCR series resonance circuit.
5. BJT input and output characteristics
6. FET Output andtransfer characteristics
7. UJT VI characteristics
8. LDR characteristics
9. IC regulated power supply(IC-7805)

Lab experiments are to be done on breadboard and simulation software (using multisim) and output values are to be compared and justified for variation.

Scheme of Evaluation

Practicals :-50 Marks

Formula & Explanation:	**6**
Tabular Form+Graph+Circuit Diagram:	**6**
Observations:	**12**
Caluclation,Graph, Precautions& Result:	**6**
Viva-Voce:	**10**
Record:	**10**

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FIRST SEMESTER END EXAMINATIONS
I B.Sc. – CIRCUIT THEORY AND ELECTRONIC DEVICES

w.e.f (2025-26) Admitted Batch

(25ELE12)

Time : 3hours Max.Marks:60.

Answer any five questions from Section A & Section B choosing at least two from each section.

Eachquestion carries 8 marks. **5x8=40 marks**

Part – 1

Section-A

1. Derive the expressions for Average value and RMS value of AC current.

2. Explain the V-I phase relation for the circuit containing R, L and C.

3. State and prove maximum power transfer theorem?

4. State and prove Thevenin's theorem.

5. Deduce expressions for resonant frequency and Q-factor for a Series resonant circuit.

Section-B

6. Obtain the expressions for resonant frequency and Q-factor for a Parallel resonant circuit.

7. Draw and explain input and output characteristics of transistor in CE configuration.

8. Explain the working and characteristics of FET.

9. Explain the working of Full wave Bridge rectifier and find its ripple factor.

10. Explain the construction and working of LED. Mention its applications

Part – 2

SECTION- C

Answer any five questions. **5x4=20 marks**

11. Explain current and voltage.
12. Difference between AC and DC.
13. State and prove Superposition theorem.
14. Explain Star to Delta and Delta to Star conversion.
15. Describe the working of RC circuit as Integrator.
16. Explain about RL as a low pass filter.
17. What are the advantages of FET over BJT?
18. Explain the working of L-section filter.

THE BLUEPRINT FOR SEE

Part-1: Answer any five questions choosing at least two from each Section A & Section B.

Each question carries 8 marks. 5x8=40 marks

Part-2: Answer any five questions. Each question carries 4 marks. 5x4=20 marks

Unit	Part-1		Part-2	Total Marks
	Section-A	Section-B		
Unit I	2		2	24
Unit II	2		2	24
Unit III	1	1	2	24
Unit IV		2	1	20
Unit V		2	1	20
	5	5	8	112

(University Nominee) (Subject Expert)

(Subject Expert) (Head Of the Department)

(Alumni) (Industrialist)

S.V.K.P. & Dr. K.S. Raju Arts & Science College (Autonomous),

PENUGONDA

II -Semester Electronics Major -1

Course1: Semiconductor devices and materials (25ELE21)

(w.e.f. 2025-26 AB)

THE BLUEPRINT FOR CIA

Section-A: Answer any three questions out of five questions.

Each question carries 6 marks. 3x6=18 marks

Section-B: Answer any three questions out of five questions.

Each question carries 4 marks. 3x4=12 marks

Mid Term Examination – I					
Unit	**Section-A**	**Section-B**	**Co-Curricular Activity**	**Extra-Curricular Activity**	**Total Marks**
Unit I	2	2	5	5	40
Unit II	2	2			
Unit III	1	1			
Total	5(3X6=18M)	5(3X4=12M)			
Mid Term Examination – II					
Unit	**Section-A**	**Section-B**	**Co-Curricular Activity**	**Extra-Curricular Activity**	**Total Marks**
Unit III	1	1	5	5	40
Unit IV	2	2			
Unit V	2	2			
Total	5(3X6=18M)	5(3X4=12M)			

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PENUGONDA-534 320, West Godavari District., (A.P.)

SEMESTER-II Syllabus w.e.f (2025-2026)

MAJOR 1

COURSE 3 : SEMICONDUCTOR DEVICES AND MATERIALS

(25ELE21)

Objective:

1. To provide basic knowledge and concepts of Semiconductor materials and devices.
2. To facilitate students learn on the physical principles and operational characteristics of Semiconductor devices and some of it's important applications. Pre-requisites: Basic Understanding of semi conductors.

Outcomes:

Materials for electronic device application in modern electronic industry.

- Detailed knowledge of various classifications and applications to VLSI, LEDs and solar cells.
- Holistic view of the latest progress in two-dimensional (2D)-one-dimensional (1D) and nano materials.

Unit I semiconductor and its classification (9HRS)

Classification of materials, classification of semi conductor materials, crystal structure and Bonding in semi conductors Intrinsic and extrinsic semiconductors, energy bands and charge Carriers, carrier transport mobility drift and diffusivity and recombination.

Unit II PN junctions (9HRS)

PN junction diode**,** Forward and reverse bias characteristics, junction capacitance and break down mechanism , Zener diode V-I characteristics, LED V-I characteristics, Zener diode acts as voltage regulator .

Unit III Field effect transistors (FET) (9HRS)

Field effect transistor (FET), junction FET(JFET),MOSFET structures and device characteristics,Applications of MOSFET, Charge coupled devices (CCD's), Applications to VLSI.

Additional Topic: - Applications of CCD for memory devices.

Unit IV Nonvolatile Memory Device (9HRS)

Optoelectronic Devices: solar cell, photo detectors, LEDs, laser diodes. Nano structures and concepts: quantum wells, supper lattice structures , Nano rod, quantum dot, CNTs, 2D materials: graphene, MoS2 etc, Mata materials.

Additional Topic: - Applications of Quantum dots .

UNIT-V Multistage Amplifiers (9HRS)

BJT at high frequencies, frequency response of RC coupled amplifiers and transformer coupled amplifier.

Reference Books:-

1. Donald A. Neamen, Semiconductor Physics and Devices Basic Principles, 3rdedn.McGraw-Hil (2003)
2. B.G. Streetman and Sanjay Banerjee, Solid State Electronic Devices, 6thEdn., Prentice Hall, 2006.
3. S. M. Sze and Kwok K. Ng Physics of Semiconductor Devices, Wiley (2013).
4. M. Hussa, A. Dimoulas and A. Molle, 2D Materials for Nano Electronics, CRC press(2016)

SEMESTER-II

Practical Paper

Work load: 30 Hrs per semester 2hrs\Week.

Minimum of 6 Experiments to be done and Recorded.

List of Experiments :-

1. To study the Hall Effect: determine the Hall coefficient, type of semiconductor And carrier concentration in the given semiconductor sample.
2. To study the four probe method: calculate the resistivity and energy band gap of given semiconductor sample.
3. To determine the resistivity of the given semiconductor specimen using Vander Pauw method.
4. To design a MOSFET as switching regulator for given duty cycle and plot the Current-voltage (I-V) characteristic of MOSFET using Keithley.
5. To design a phase controlled rectifier using SCR and plot the I-V characteristic Of SCRusing Keithley.
6. To design a relaxation oscillator using UJT and plot the I-V characteristic of UJT using Keithley.
7. I-V characteristics measurement of a p-n diode/LEDs using Keithley - calculate It's ideality factor.

Scheme of Evaluation

Practical's :-50 Marks

Formula & Explanation:	**6**
Tabular Form+Graph+Circuit Diagram:	**6**
Observations:	**12**
Caluclation,Graph,Precautions& Result:	**6**
Viva-Voce:	**10**
Record:	**10**

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SECOND SEMESTER END EXAMINATIONS

I B.Sc. –ELECTRONICS –MAJOR1/MINOR SEMICONDUCTOR DEVICES AND MATERIALS

w.e.f 2025-26 admitted batch Model paper(23ELE21)

Time : **3hours** Max.Marks:**60.**

Answer any five questions from Section A& Section B choosing atleast two from each section.

Eachquestion carries 8 marks. **5x8=40 marks**

Part – 1

Section-A

1. Explain the concept of drift and diffusivity in semiconductors ?
2. Explain the classification of semiconductors ?
3. what is P-N junction diode ?Explain the V-I characteristics of P-N junction diode ?
4. What is zenar diode ? Explain Zenar diode act as a voltage regulator ?
5. write about field effect transistor (FET) ?

Section-B

6. Explain construction and working of MOSFET?

7. Explain the operational principle of LED's and write its V-Icharacteristics?

8. Explain the principle and working of solar cell ?

9. Explain the concept of transformer coupling in amplifiers?

10. Explain construction and working of RC coupled amplifier ?

Part – 2

SECTION- C

Answer any five questions. Each question carries 4 marks **5x4=20marks**

11. Explain the energy bands in a semiconductor?
12. What is meant by carrier transport?
13. What is break down mechanism?
14. Write about charge coupled devices (CCDs) ?
15. Write a short note on CNT's?
16. What are the applications of VLSI?
17. What is meant by QUANTUM DOTS?
18. Explain operation of bipolar junction transistor?

THE BLUEPRINT FOR SEE

Part-1: Answer any five questions choosing at least two from each Section A & Section B.

Each question carries 8 marks. 5x8=40 marks

Part-2: Answer any five questions.

Each question carries 4 marks. 5x4=20 marks

Unit	Part-1		Part-2	Total Marks
	Section-A	Section-B		
Unit I	2		2	24
Unit II	2		1	20
Unit III	1	1	2	24
Unit IV		2	2	24
Unit V		2	1	20
	5	5	8	112

(University Nominee) (Subject Expert)

(Subject Expert) (Head Of the Department)

(Alumni) (Industrialist)

S.V.K.P. & Dr. K.S. Raju Arts & Science College (Autonomous),

PENUGONDA

II -Semester Electronics Major -2

Course 2: Digital Electronics (25ELE22)

(w.e.f. 2025-26 AB)

THE BLUEPRINT FOR CIA

Section-A: Answer any three questions out of five questions.

Each question carries 6 marks. 3x6=18 marks

Section-B: Answer any three questions out of five questions.

Each question carries 4 marks. 3x4=12 marks

Mid Term Examination – I					
Unit	**Section-A**	**Section-B**	**Co-Curricular Activity**	**Extra-Curricular Activity**	**Total Marks**
Unit I	2	2	5	5	40
Unit II	2	2			
Unit III	1	1			
Total	5(3X6=18M)	5(3X4=12M)			
Mid Term Examination – II					
Unit	**Section-A**	**Section-B**	**Co-Curricular Activity**	**Extra-Curricular Activity**	**Total Marks**
Unit III	1	1	5	5	40
Unit IV	2	2			
Unit V	2	2			
Total	5(3X6=18M)	5(3X4=12M)			

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(Affiliated to ADIKAVI NANNAYA UNIVERSITY - Recognised by Govt. of Andhra Pradesh)
PENUGONDA-534 320, West Godavari District., (A.P.)

SEMESTER-II Syllabus w.e.f (2025-2026)

MAJOR - II

COURSE 4: DIGITAL ELECTRONICS

(25ELE22)

Objectives:

- To understand the number systems, Binary codes and Complements.
- To understand the Boolean algebra and simplification of Boolean expressions.
- To analyze logic processes and implement logical operations using combinational logic circuits.
- To understand the concepts of sequential circuits and to analyze sequential Systems in terms of state machines.
- To understands characteristics of memory and their classification.
- To implement combinational and sequential circuits using VHDL.

Unit – I NUMBER SYSTEM AND CODES (9HRS)

Decimal, Binary, Hexadecimal, Octal. Codes:BCD, Gray and Excess-3 codes-code conversions- Complements (1's, 2's, 9's and10's), Addition -Subtraction using complement methods.

Additional topic: - Significance of parity

Unit- II BOOLEAN ALGEBRA AND THEOREMS (9HRS)

Boolean Theorems, De-Morgan's laws. Digital logic gates, Multi level NAND & NOR gates. Standard representation of logic functions (SOP and POS), Minimization Techniques(Karnaugh Map Method: 2,3 variables).

UNIT-III COMBINATIONAL DIGITAL CIRCUITS (9HRS)

Adders-Half & full adder, Subtractor -Half and full subtractors, Parallel binary adder, Magnitude Comparator, Multiplexers (4:1)) and Demultiplexers (1:4), Encoder (8-line-to-3- line) and Decoder (3-line-to -8-line). IC-LOGIC FAMILIES: TTL logic, CMOS Logic families (NAND&NOR Gates).

UNIT-IV SEQUENTIAL DIGITAL CIRCUITS (9HRS)

Flip Flops: S-R FF, J-K FF, T and D type FFs, Master-Slave FFs, Excitation tables, Registers:- Serial In Serial Out and Parallel In and Parallel Out, Counters Asynchronous-, Mod-8,Mod- 10,Synchronous-4-bit &Ring counter.

Additional Topic: - conversion of Flip Flops

UNIT- V MEMORYDEVICES (9HRS)

General Memory Operations, ROM, RAM (Static and Dynamic), PROM, EPROM,EEPROM, EAROM,

Outcomes:-

- develop a digital logic and apply it to solve real life problems.
- Analyze, design and implement combinational logic circuits.
- Classify different semiconductor memories.
- Analyze, design and implement sequential logic circuits.
- Simulate and implement combinational and sequential logic circuits using VHDL

TEXT BOOKS:-

1 . M.Morris Mano, " Digital Design " 3rd Edition, PHI, NewDelhi.

2. Ronald J. Tocci. "Digital Systems-Principles and Applications" 6/e. PHI. New Delhi.1999.(UNITS I to IV)

3. G.K.Kharate-Digital electronics-oxford university press

4.S.Salivahana& S. Arivazhagan-Digital circuits and design

5.Fundamentals of Digital Circuits by Anand Kumar

6.Digital Electronics-Deepak Garge, ,Pragathiprakasan, Meerut

REFERENCE BOOKS :-

1.Herbert Tauband Donald Schilling."Digital Integrated Electronics".McGraw Hill.1985.

2.S.K. Bose. "Digital Systems".2/e.New Age International.1992.

3.D.K. Anvekar and B.S. Sonade. "Electronic Data Converters : Fundamentals &Applications".TMH. 1994.

4. Malvino and Leach. " Digital Principles and Applications". TMG HillEdition

SEMESTER-II

Practical Paper: DIGITAL ELECTRONICS LAB

Work load: 30 Hrs per semester 2hrs\Week.

Minimum of 2 Experiments to be done and Recorded.

Course Outcomes:

1. Develop a digital logic and apply it to solve real life problems.
2. Analyze, design and implement combinational logic circuits.
3. Classify different semiconductor memories.
4. Analyze, design and implement sequential logic circuits.

List of the Experiments:-

1. Verification of IC-logic gates
2. Realization of basic gates using discrete components (resistor, diodes &transistor)
3. Realization of basic gates using Universal gates (NAND &NOR gates)
4. Verification of Half adder and Full adder circuits using gates
5. Verification of Half subtractor and Full subtractor using gates.
6. Verification of truth tables- Multiplexer and De-multiplexer.
7. Verification of truth tables- Encoder and decoder.
8. Verification of truth tables- RS , JK, T-F/F using NAND gates
9. 4-bit binary parallel adder and subtractor using IC7483
10. BCD to seven segment decoder using IC -7447/7448

Scheme of Evaluation

Practical's :-50 Marks

Formula & Explanation:	**6**
Tabular Form+Graph+Circuit Diagram:	**6**
Observations:	**12**
Caluclation,Graph, Precautions& Result:	**6**
Viva-Voce:	**10**
Record:	**10**

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SECOND SEMESTER END EXAMINATIONS

I B.Sc. –ELECTRONICS –DIGITAL ELECTRONICS (25ELE22)

w.e.f (2025-26) Admitted Batch

MODEL PAPER

Time : 3hours **Max.Marks:60.**

Answer any five questions from Section A& Section B choosing at least two from each section.

Eachquestion carries 8 marks. **5x8=40 marks**

Part – 1

Section-A

1. Explain in detail about BCD Code?
2. Explain the conversion of Decimal to Binary and binary to decimal with an example?
3. Why NAND and NOR gates are universal gates? Realize AND, OR and NOT gates using NAND and NOR gates ?
4. Explain in detail about 3 variable karnaugh map method to simplify logic Expression?
5. Explain the operation of a full adder circuit with its truth table?

Section-B

6. Explain the working of TTL NAND Gate circuit with its truth table?
7. Describe the working of Master slave JK flip-flop with its truth table?
8. Draw the circuit diagram of decade counter and explain it's operation. Draw its Timing diagram?
9. Explain the operation of ROM?
10. Explain the operation of Dynamic RAM?

Part – 2

SECTION- C

Answer any five questions. Each question carries 4 marks 5x4=20 marks

11. Explain Excess-3 codes with an example.
12. Subtract 11001 from 10101 using 2's complement method
13. Prove the Boolean identity (AB +C) (AB +D) = AB + CD
14. State and prove Demorgan's law's.
15. Write down differences between CMOS and TTL logic families.
16. Explain the working of Multiplexer (4:1) with its truth table.
17. Explain the operation of RS flip – flop with truth table
18. Explain EPROM and EEPROM in brief.

THE BLUEPRINT FOR SEMESTER END EXAMSINATIONS (SEE)

Part-1: Answer any five questions choosing at least two from each Section A & Section B.

Each question carries 8 marks. 5x8=40 marks

Part-2: Answer any five questions. Each question carries 4 marks. 5x4=20 marks

Unit	Part-1		Part-2	Total Marks
	Section-A	Section-B		
Unit I	2		2	24
Unit II	2		2	24
Unit III	1	1	2	24
Unit IV		2	1	20
Unit V		2	1	20
	5	5	8	112

(University Nominee) (Subject Expert)

(Subject Expert) (Head Of the Department)

(Alumni) (Industrialist)